LA-UR-82-837

Conf-820708--2

Los Alamos National Laboratory is operated by the University of California for the United States Department of Energy under contract W-7405-ENG-36.

LA-UR--82-837

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TITLE: ONE GIGASAMPLE PER SECOND TRANSIENT RECORDER: A PERFORMANCE DEMONSTRATION

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SUBMITTED TO: 1982 IEEE Annual Conference on Nuclear and Space Radiation Effects, Las Vegas, NV, July 20-22, 1982

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ONE GIGASAMPLE PER SECOND TRANSIENT RECORDER: A PERFORMANCE DEMONSTRATION*

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ABSTRACT--The performance demonstrated by a one gigasample per second (1 Gs/s) transient recorder currently in advanced development portends an important new instrument for recording single transient data. A Charge-Coupled Device (CCD) is used to sample a continuous analog signal. Samples acquired at the full sampling rate (1 Gs/s) are temporarily stored in the CCD, then read out at a slow rate (e.g., 250 Ks/s) into a conventional analog-to-digital converter prior to storage in nonvolatile, digital memory. Enhanced circuitry and techniques developed over the past three years have yielded higher performance than originally anticipated. Accordingly, the target specification shown in Figure 1 has been revised to reflect higher expectations.

BACKGROUND--Some aspects of testing nuclear weapons and their effects require high dynamic range and wide-bandwidth coupled with considerable post-acquisition data processing. Oscilloscope traces recorded on photographic film and subsequently digitized have been the workhorse of this activity. Since the data is to be processed digitally, there are compelling arguments (e.g., cost, accuracy and error management) for converting the continuous, analog phenomena to a digital form as early in the process as possible. However, conventional means of analog-to-digital conversion do not function at 1 Gs/s with 10-bit resolution with DC-200 MHz bandwidth. Clearly, an unconventional approach was in order. Acknowledging similar recording requirements, LANL and LLNL agreed to collaborate on a CCD-based transient recorder. Q-DOT, Inc. was retained to develop the recorder. LLNL agreed to develop the CCD. EG&G planned to evaluate hardware performance and eventually field completed systems.

The recorder centers around a CCD configured as five parallel, analog, shift registers. Each shift register has a high-precision, wide-bandwidth signal sampler and stores 128 data samples. The five registers are clocked synchronously at rates up to 200 Ms/s yielding a sample every 5 ns on each register. The CCD can acquire 128 samples of five independent data channels. Alternatively, the same data can

*Part of this work was performed by Q-DOT, Inc. under subcontract to Los Alamos National Laboratory (LANL). Other parts were performed by EG&G, Inc. and Lawrence Livermore National Laboratory (LLNL). LANL, EG&G, and LLNL are all prime contractors of the U.S. Department of Energy (DOE).

be applied to several registers to obtain more samples at faster sampling rates. The principal application employs all five registers for one data channel. Data is split into a series of five successively longer paths. An incremental path length of 1 ns combined with 5 ns sampling on each register produces continuous 1 ns (i.e., 1 Gs/s) samples. After their acquisition, samples are clocked out of the five shift registers at a slow rate (e.g., 50 Ks/s) into a common output shift register, through a common analog-to-digital converter into digital memory.

The basic system was reported in the IEEE Transactions in Nuclear Science[1] in 1979. At that time, the basic hardware had been integrated and delivered but not evaluated. In the past three years, all aspects of the systems have been thoroughly evaluated. Significant improvements were implemented. This paper will relate key improvements to performance parameters and report current performance relative to the target specification.

IMPROVEMENTS--Several improvements have been incorporated in the transient recorder design since it was initially reported in 1979. These include:

Reference register deleted: The original CCD design was configured as four data registers plus an identical reference register. The reference register was intended to aid in post-acquisition data corrections. In fact, it is not necessary for that function and is now used as another data register. This increased the CCD's capacity from 512 samples to 640 samples.

CCD driven with two-phase clocks: For initial characterization, the CCD was driven with a series of four clocks each shifted 90° in phase from the next. Tests with two clocks shifted 180° apart yielded nearly equivalent CCD performance. Since a two-phase system operates with fewer CCD clock drivers, fewer I/- connections to the CCD, and simpler timing circuitry, it was adopted.

Time base subharmonics reduced: Subharmonics in the time base cause the instant of sampling to vary in a fixed pattern. This error can potentially be measured and subsequently taken into account in data reduction. However, it is better eliminated. By carefully isolating potential subharmonic sources from the time base circuitry, all subharmonics are now below 60 dB and are not observed as timing error in the recorded data.

Post-acquisition data correction enhanced: Drift in the CCD and close support circuitry is consistently less than 0.1% of full scale. Drift on this order permits detailed, accurate characterization of operations that various circuit elements perform on the data as it passes through them. With adequate processing power, the influence of the operations on the data can be minimized, sometimes to insignificant levels. Given the demonstrated system stability, an Intel 8086 microprocessor with the 8087 mathematics co-processor was chosen to permit extensive post-acquisition data manipulation. The 8086/8087 operates with 80-bit floating-point words (19 digit precision) under FORTRAN at rates to 0.015 Megaflops/second.

Programmable signal offset added: One of the methods considered for remotely calibrating part of the system also offered the ability to locate signal ground at any point in the full scale range of the instrument. After discussion with users, this feature was incorporated in the system.

Several other features were also added, including, error corrected memory and the ability to closely synchronize several recorders. Prehistory resolution and range were both extended.

PERFORMANCE--At this writing (March, 1982), several key performance parameters have been demonstrated.

Bandwidth: The measured amplitude response is -3 dB typically between 700 MHz and 1 GHz. The roll-off is smooth (i.e., free of sharp peaks and valleys) to 2 GHZ. At 2 GHz it is typically -15 dB to -20 dB. The smooth roll-off suggests a well behaved phase characteristic.

Dynamic range (noise limited): Dynamic range is defined for this instrument as rms error to peak-to-peak signal. As such, it is intended to be an overall measure of system accuracy. A limiting component of this error is random noise. The signal-to-noise (rms) ratio typically observed is 60 dB. This allows 10 dB margin for other errors combined.

Linearity: Total system non-linearity (defined as integral non-linearity, the most stringent definition) is typically less than 0.1% after post-acquisition correction.

Aperture: This is the effective signal averaging period during sampling. Given a track-and-hold sampler, it is difficult to define precisely. If the averaging process which occurs as the sampler shifts from track to hold is approximated as a window integration, the effect window is typically 0.2 ns.

Aperture uncertainty: The random variation in the instant of signal sampling is called aperture uncertainty. Aperture uncertainty of 1.8 ps (rms) has been demonstrated.

Sampling interval: Sampling at 1 Gs/s is routine.

The presentation in July, 1982 will show graphic data of these results as well as additional data obtained in the interim.

CONCLUSION--Recorder performance demonstrated to date offers considerable hope that the ultimate system will meet the entire target specification in the field. In fact, some specifications (e.g., system bandwidth) have been sufficiently exceeded to suggest the possibility of instruments with even higher performance.

REFERENCE--[1]Linnenbrink, T.E., Gradl, D.A., Metzger, D.S., Hodson, E.K., Thayer, D.R., DeWitte, G.J., Balch, J.W., McConaghy, C.F., "A One Gigasample Per Second Transient Recorder," IEEE Transactions on Nuclear Science, vol. NS-26, No. 4, pp. 4443-4449, August, 1979.

FIGURE 1: TARGET SPECIFICATION

Parameter	Revised (July 13, 1981)	Original (August 3, 1977)
Sampling	1 ns, 2 ns, 4 ns, 8 ns	Same
Signal BW[1]	DC-200 MHz, DC-100 MHz, DC-50 MHz, DC-25 MHz, (-3 dB)	Same
Control	Remote computer controlled, IEEE 488 RS232C (variable baud rate including 300 and 9600 baud), and front panel	Remote, computer controlled (CAMAC/HPIB) desirable
Relative accuracy[2]	10 bits, minimum	8 bits, minimum
Dynamic range[3]	50 dB, minimum	40 dB, minimum
Linearity	Reproducible, correctable to ± 0.2%	Same
Aperture[1]	Sampling interval, maximum	Same
Aperture uncertainty	± 3 ps, maximum	± 25 ps, maximum
Amplitude F.S.	± 2 V (4 Vpp), tapped delay line; ± 10 V (20 Vpp), resistive split	± 1 V (2 Vpp)
Number of samples	640, maximum (5 channels of 128)	256, minimum; 512, maximum
Number of independent data records	1 to 5	Not specified
Cross timing	± 100 ps	Same
Trigger	External, NIMS, fixed threshold (0-800 mV, 16 ma into 50Ω)	Same
Pre-history	± 640 samples, 10-sample increments, remotely programmable	0, 16, 32, 64 samples
Crosstalk	Resultant error less than other system errors	Same
Offset, common	± fullscale, increment per 14-bit (minimum) DAC, remotely programmable	Not specified
Temperature:		
Operating	50-100°F	Same
Cal to run	± 2°F	Same
Warm-up time	½ hour, minimum	Same
Memory and status register	Independent, redundant; single-bit error correction, two-bit error detection, non-volatile for 5 days	Non-volatile for 5 days
Cooling	Forced air	Same
Power monitor	Tolerance band on power supplies and batteries	Not specified
Automatic power-up recovery	Full operation	Not specified
Automatic configuration/maintenance	Module identification	Not specified

[1] Corresponds to sampling interval
[2] Resolution, resolvable elements
[3] RMS error to peak-to-peak signal